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EXAMINER	
CHHAYA, SWAPNEEL	

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
04/17/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/554,067	EL-FARHANE, REBHA	
	Examiner	Art Unit	
	SWAPNEEL CHHAYA	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/7/2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Wieczorek et al. (U.S. Patent 6274894).

Regarding claim 1. A semiconductor device comprising:

a gate electrode (44) (Fig. 10 column 9 lines 40-45) and

a gate insulating layer (42) produced on a part of the surface of a substrate (40) of a first semiconductor material having a given melting point, and surrounded by an insulating spacer (50) in a plane parallel to the surface of the substrate, (Fig. 10 column 9 lines 26-35 column 10 lines 35-45)

the gate insulating layer being disposed between the substrate and the gate electrode (Fig. 10)

a source region and a drain region (60) situated under the surface of the substrate at the level of two opposite sides of the gate electrode respectively, each region containing electrical carriers of the same given type, with respective first concentrations, and

each region comprising a portion of a second semiconductor material (56) disposed on the substrate below the level of the gate insulating layer in a direction perpendicular to the surface of the substrate, (Fig. 10 column 13 lines 20-45)
each portion of second material extending at least partially between the substrate and the spacer, substantially as far as a limit coming in line, in said perpendicular direction, with one side of the gate electrode (Fig. 10)
said portions of second material being doped with doping elements in order to create electrical carriers of said given type with second concentrations less than said first concentrations (Fig. 10 column 13 lines 20-45), and
said portions of second material having a melting point lower than the melting point of the first material, please note that this is inherent due to the materials used, namely the materials claimed in claim 3.

Regarding claim 2. A device as claimed in Claim 1, in which said portions of second material have an ability to absorb a light radiation greater than the absorption ability of the first material for the same light radiation, please note that this is inherent in the reference due to the materials used, namely the materials claimed in claim 3.

Regarding claim 3. A device as claimed in Claim 1, in which the first material is based on silicon and the second material is based on germanium or based on an alloy of silicon and germanium (column 9 lines 15-25, column 12 lines 15-25)

Regarding claim 6. A device as claimed in claim 1, characterized in that said device is an MOS transistor (column 7 lines 50-60).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek in view of Chau et al. (U.S. Patent 5710450).

Regarding claim 4. Wieczorek discloses the claimed invention except for the encapsulation portions disclosed on top of the portions of second material.
Chau discloses:
A device as claimed in Claim 1, also comprising two encapsulation (420) portions of said second material, disposed respectively over the portions of second material (314) on a side opposite to the substrate. (Fig. 4 column 6 lines 1-10, column 7 lines 50-60 column 8 lines 1-10)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the encapsulation portions as taught by Chau, since

Chau states at column 7 lines 60-67 column 8 line 1-2 that such a modification would facilitate an adequate source/drain contact region for the fabricated device. .

Regarding claim 5. Chau discloses:

A device as claimed in Claim 4, in which each encapsulation portion extends between the spacer and the portion of second material above which said encapsulation portion is disposed, substantially as far as a limit situated in line, in said direction perpendicular to the surface of the substrate, with the side of the gate electrode corresponding to said second encapsulation portion. (Fig. 4 column 6 lines 1-10, column 7 lines 50-60 column 8 lines 1-10)

5. Claims 7, 8, 9, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (U.S. Patent 5710450) in view of Andideh et al. (U.S. Patent 6121100) and further in view of Wieczorek et al. (U.S. Patent 6274894).

Regarding claim 7 and 11. Chau discloses:

A method of manufacturing a semiconductor device, comprising the following *successive* steps:

a) a gate insulating layer (302) is formed on a part of a surface of a substrate (300) in a first semiconductor material having a given melting point (Fig. 3A column 4 lines 25-30)

b) a gate electrode (306) is formed on top of the gate insulating layer (Fig. 3A column 4 lines 30-35)

c) an insulating spacer (308) is formed, disposed around the gate insulating layer and the gate electrode, parallel to the surface of the substrate (Fig. 3A-3F column 4 lines 45-65)

d) two surface films of the first material are removed respectively in two lateral parts of the surface of the substrate situated on two opposite sides of the surface part of the substrate carrying the gate insulating layer and the gate electrode, each lateral part extending between the substrate and the spacer substantially as far as a limit coming in line with one of the opposite sides of the gate electrode in a direction perpendicular to the surface of the substrate (Fig. 3A-3F column 4 lines 60-67, column 5 lines 1-5)

Chau discloses the claimed invention except for the formation of the deep source/drain regions prior to the formation of the extensions.

Andideh teaches:

e) a source region and a drain region (310) are formed, each region being situated below the surface of the substrate at a level of said two electrode parts of the surface of the substrate respectively, each region containing electrical carriers of the same given type with respective first concentrations; (Fig. 3F column 8 lines 50-60)

f) there is formed on the substrate, in each lateral part a portion in a second semiconductor material (318) substantially as far as a limit coming in line, in said perpendicular direction, with the opposite side of the gate electrode corresponding to said lateral part, said portions of second material containing doping elements in order to

create electrical carders of the given type, and having a melting point lower than the melting point of the first material; (Fig. 3F-3h column 8 lines 20-65)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the deep source/drain implants prior to the formation of the source/drain extensions as taught by Andideh, since Andideh states at column 8 line 603-67 column 9 lines 1-5 that such a modification would enable a deeper implant using relatively low energy.

Chau in view of Andideh discloses the claimed invention except for the heating of the portions of the second material.
Wieczorek discloses:
g) the portions of second material are heated to a temperature intermediate between the respective melting points of the first and second materials, so that the portions of second material contain electrical carriers with second concentrations lower than said first concentrations.(column 13 lines 20-45)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to heat the portions of the material as taught by Wieczorek, since Wieczorek states at column 13 line 35-45 that such a modification would activate the impurities and repair damage to the substrate.

Regarding claim 8.

Chau in view of Andideh and further in view of Wieczorek discloses the claimed invention except for use of a laser to heat the portions of the material.
A method as claimed in Claim 7, according to which, during step g), said portions of second material are heated using a laser beam.
However, It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the laser since it was known in the art that a laser can be used to anneal a source and/or a drain in order to activate dopants. The use of a laser to anneal a source and drain is disclosed in the abstract of Puchner (U.S. Patent 6358806).

Regarding claim 9. Chau discloses:
A method as claimed in Claim 7, according to which, after step f), encapsulation (420) portions are deposited respectively on top of said portions of second material, on a side opposite to the substrate. (Fig. 4 column 6 lines 1-10, column 7 lines 50-60 column 8 lines 1-10)

Regarding claim 10. Chau in view of Andideh and further in view of Wieczorek does not disclose A method as claimed in Claim 7, according to which step e) is performed before step d).

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to perform the steps in the order claimed in claim 10 because Applicant has not disclosed that implementing the steps in

this order provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected the invention of Chau in view of Andideh and Wieczorek, and applicant's invention, to perform equally well with either the order claimed in claim 7 or the order claimed in claim 10 because both would perform the same function of a semiconductor device, namely a transistor.

Therefore, it would have been prima facie obvious to modify Chau in view of Andideh and further in view of Wieczorek to obtain the invention as specified in claim 10 because such a modification would have been considered a mere design consideration which fails to patentably distinguish over the prior art.

Response to Arguments

6. Applicant's arguments filed 1/7/2008 have been fully considered but they are not persuasive.

7. Applicant argues:

Applicant respectfully traverses the Section 102(b) rejection of claims 1-3 and 6 because the cited portions of the Wieczorek reference do not correspond to the claimed invention which includes, for example, aspects directed to each portion of second semiconductor material extending between the substrate and the spacer substantially

as far as a limit coming in line with one side of the gate electrode in the perpendicular direction. The Office Action erroneously asserts that Wieczorek's semiconductor portions 56 correspond to the claimed portions of second semiconductor material. However, the cited portions of Wieczorek teach that trenches 52 are self aligned to sidewalls of encapsulated gate conductor 44 (specifically, to sidewalls of dielectrics 50), and the remaining portions of trenches 52 are filled with portions 56. See, e.g., Figure 7 and 9; Col. 10:52-59 and Col. 12:16-17. As is clearly shown in Wieczorek's Figure 9 (reproduced below with the sidewalls of gate conductor 44 highlighted), semiconductor portions 56 do not extend to the sidewalls of gate conductor 44 as do the portions of second semiconductor material of the claimed invention (see, e.g., Applicant's Figure 1). Instead, Wieczorek's semiconductor portions 56 only extend to the sidewalls of dielectrics 50 since the trenches 52 (in which portions 56 are formed) are self aligned to the sidewalls of dielectrics 50. Therefore, Wieczorek's semiconductor portions 56 do not correspond to the claimed portions of second semiconductor material. Accordingly, the Section 102(b) rejection of claims 1-3 and 6 is improper and Applicant requests that it be withdrawn.

Applicant's arguments are not commensurate with the scope of applicant's claims. Furthermore, it is understood that the drawings of references are not drawn to scale. Applicant claims that "each portion of second material extending at least partially between the substrate and the spacer substantially as far as a limit coming in line, in said perpendicular direction with one side of the gate electrode. "Applicant's argues that

since the trenches which are subsequently filled with semiconductor portions 56 are self aligned to "sidewalls of dielectrics 50" that it does not meet the limitation. It is entirely possible that the trenches could be aligned to the inner sidewalls of dielectrics 50 which would mean that they would extend directly to the gate conductor.

Another aspect of applicant's claimed invention is the term "substantially" which dictates that the semiconductor portions extend considerably towards the gate conductor. That aspect, when combined with applicant's Figure 7 which shows portions 8 and 9 extending substantially towards the gate conductor, render applicant's arguments to not be commensurate with applicant's claimed invention.

8. Applicant argues:

Applicant further traverses the Section 103(a) rejection of claim 5 because the cited portions of the Chau reference do not correspond to aspects of the claimed invention directed to each encapsulation portion extending between the spacer and the portion of second semiconductor material above which said encapsulation portions is deposited. The Office Action erroneously asserts that Chau's second semiconductor material 420 corresponds to the claimed encapsulation portions. However, as is clearly shown by Chau in Figure 4, Chau's second semiconductor material 420 does not extend between semiconductor material 314 and sidewall spacer 318. Thus, Chau's second semiconductor material 420 does not correspond to the encapsulation portions of the

claimed invention. Accordingly, the Section 103(a) rejection of claim 5 is improper and Applicant requests that it be withdrawn.

Applicant's arguments are not commensurate with the scope of applicant's claims. Furthermore, it is understood that the drawings of references are not drawn to scale. Applicant claims that "each portion of second material extending at least partially between the substrate and the spacer substantially as far as a limit coming in line, in said perpendicular direction with one side of the gate electrode. "
One aspect of applicant's claimed invention is the term "substantially" which dictates that the semiconductor portions extend considerably towards the gate conductor. That aspect, when combined with applicant's Figure 7 which shows encapsulation portions 8 and 9 extending substantially towards the gate conductor, render applicant's arguments to not be commensurate with applicant's claimed invention.

9. Applicant argues:

Applicant respectfully traverses the Section 103(a) rejection of claims 7-10 because the cited portions of the Chau reference do not correspond to the claimed invention which includes, for example, aspects directed to removing two lateral parts of the first semiconductor material with each lateral part extending between the substrate and the spacer up to the opposite sides of the gate electrode. As is clearly shown by Chau in Figure 3B, the recesses 312 formed by Chau in substrate 300 do not extend

between substrate 300 and spacers 310 and the recesses 312 also do not extend up to the sidewalls of gate electrode 306. Thus, the cited portions of the Chau reference do not correspond to the claimed invention. Accordingly, the Section 103 (a) rejection of claims 7-10 is improper and Applicant requests that it be withdrawn.

Applicant's arguments are not commensurate with the scope of applicant's claims. Furthermore, it is understood that the drawings of references are not drawn to scale. Applicant claims that "each portion of second material extending at least partially between the substrate and the spacer substantially as far as a limit coming in line, in said perpendicular direction with one side of the gate electrode."""
One aspect of applicant's claimed invention is the term "substantially" which dictates that the semiconductor portions extend considerably towards the gate conductor. That aspect, when combined with applicant's Figure 7 which shows encapsulation portions 8 and 9 which are recesses corresponding to those in the rejection of claims 7-10, that were subsequently filled, extending substantially towards the gate conductor, render applicant's arguments to not be commensurate with applicant's claimed invention.

10. Applicant argues:

Applicant further traverses the Section 103 (a) rejection of claims 7-10 because the cited portions of the Andideh reference do not correspond to the claimed invention which includes, for example, aspects directed to in each lateral part, forming a portion of

a second semiconductor material that extends up to the opposite sides of the gate electrode. As is clearly shown by Andideh in Figure 3B, semiconductor material 318 does not extend up to the sidewalls of gate electrode 306; instead Andideh teaches that semiconductor material 318 only extends up to spacer 314 which is formed along the sidewalls of gate electrode 306. Thus, the cited portions of the Andideh reference do not correspond to the claimed invention. Accordingly, the Section 103 (a) rejection of claims 7-10 is improper and Applicant requests that it be withdrawn.

Applicant's arguments are not commensurate with the scope of applicant's claims. Furthermore, it is understood that the drawings of references are not drawn to scale. Applicant claims that "each portion of second material extending at least partially between the substrate and the spacer substantially as far as a limit coming in line, in said perpendicular direction with one side of the gate electrode."
One aspect of applicant's claimed invention is the term "substantially" which dictates that the semiconductor portions extend considerably towards the gate conductor. That aspect, when combined with applicant's Figure 7 which shows semiconductor material 8 and 9 extending substantially towards the gate conductor, render applicant's arguments to not be commensurate with applicant's claimed invention.

11. Applicant argues:

Applicant further traverses the Section 103(a) rejection of claims 7-10 because the

cited portions of the Wieczorek reference do not correspond to the claimed invention which includes, for example, aspects directed to heating the portions of second semiconductor material to a temperature that is between the melting points of the first and second semiconductor materials. The cited portions of Wieczorek simply teach that an anneal is performed. See, e.g., Col. 13:20-45. However, these portions of Wieczorek fail to make any mention of the temperature at which the annealing is performed, much less that it is performed at a temperature that is between the melting points of first and second semiconductor materials as in the claimed invention. Thus, the cited portions of the Wieczorek reference do not correspond to the claimed invention. Accordingly, the Section 103(a) rejection of claims 7-10 is improper and Applicant requests that it be withdrawn.

Wieczorek recites in Col 13:20-45 that "An anneal is performed after implantation of portions 60 in order to activate the impurities". It is understood that applicant's claims are interpreted in light of applicant's disclosure which includes the claims, drawings, and applicant's specification. On page 6 lines 5-15 applicant recites that "This heating of the portions 6 and 7 may possibly serve simultaneously as a heating activation for the electrical carriers in the regions 4 and 5." Thus the cited portion of the Wieczorek reference implicitly anticipates the limitations of claims 7-10.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to out in whose telephone number is (571)270-1434. The examiner can normally be reached on Monday- Thursday 9:30-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/
Supervisory Patent Examiner, Art Unit 2822

SC